

REMARKS

Claims 1-4 and 6-9 are pending in this application. Claim 5 and non-elected claims 10-12 have been canceled. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment, which is captioned "Version with Markings to Show Changes Made."

Allowable Claims

Applicant gratefully acknowledges that original claims 5, 6, 8 and 9 were merely objected to as depending from a rejected base claim, but are otherwise allowable.

Rejections under 35 USC §102(b)

Claims 1-4 were rejected under 35 USC §102(b) as being anticipated by Pfiester (U.S. Patent No. 4,745,079).

Claim 1 has been amended to incorporate the recitation of original claim 5. Because original claim 5 has already been allowed by the Examiner, the amendment has placed the application in condition for allowance.

Rejections under 35 USC §103(a)

Claim 7 was rejected under 35 U.S.C. §103(a) as being obvious over Pfiester, and further in view of Onishi (U.S. Patent No. 5,856,693).

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Claim 7 depends from claim 1. Therefore, this rejection also has been overcome by the above amendment to claim 1.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with Markings to Show Changes Made

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IN THE CLAIMS:

Claim 5 has been canceled.

Claims 1 and 6 have been amended as follows:

1. (Amended) A semiconductor device, comprising:
a source region formed of a semiconductor;
a drain region formed of a semiconductor of the same conductive type as that of said source region;
a channel region formed of a semiconductor between said source region and said drain region;
a gate insulating film provided on said channel region; and
a gate electrode provided on said gate insulating film and formed with a P-N junction including a
P-type semiconductor region and an N-type semiconductor region,
wherein said P-type semiconductor region and said N-type semiconductor region of said P-N
junction of said gate electrode are electrically insulated,
wherein said gate electrode includes a first gate portion provided above said channel region and
a second gate portion provided above a region which is not said channel region, and said second gate
portion includes said P-N junction.

6. (Amended) The semiconductor device according to ~~claim 5~~ claim 1, further comprising;

a body region formed of a semiconductor under said channel region;

a buried insulating film provided under said body region, said source region, and said drain region;

and

a semiconductor substrate region provided under said buried insulating film.